WHAT IS CLAIMED IS:

1. An interband tunnel diode, comprising:

a bottom injector;

a bottom spacer;

a top spacer;

a top injector formed adjacent to, but not necessarily in direct contact with, the bottom injector, the bottom injector and top injector layers forming a p-n junction; and

a material inserted between the bottom injector and top injector which serves as a tunnel barrier.

2. The interband tunnel diode as recited in claim 1, wherein the layers in the interband tunnel diode are a semiconductor or insulator.

3. The interband tunnel diode as recited in claim 1, wherein the layers in the interband tunnel diode are a Si compatible material.

4. The interband tunnel diode as recited in claim 1, wherein the layers in the interband tunnel diode are comprised of a Group IV alloy.

5. The interband tunnel diode as recited in claim 1, wherein the layers in the interband tunnel diode are comprised of, but not limited to, Si, Ge, C, Sn, $Si_{1-x}Ge_x$, $Si_{1-x}C_x$, $Si_{1-x}Sn_x$, $Si_{1-x-y}Ge_xC_y$, $Si_{1-x-y-z}Ge_xC_ySn_z$, $Si_{1-x}O_x$, $Si_{1-x}N_x$, $Al_{1-x}O_x$, or combinations thereof.

6. The interband tunnel diode as recited in claim 1, wherein the tunnel barrier material is doped below 10^{17} cm^{-3}.

7. The interband tunnel diode as recited in claim 1, wherein the tunnel barrier is less than or equal to 50 nm thick.

8. The interband tunnel diode as recited in claim 1, wherein the tunnel barrier is less than or equal to 10 nm thick.

9. The interband tunnel diode as recited in claim 1, wherein the doping concentrations of the top and bottom injector layers are between 1×10^{15} cm^{-3} and 5×10^{22} cm^{-3}, and not necessarily equal.

10. The interband tunnel diode as recited in claim 1, wherein the top and bottom spacer layers are doped below 10^{17} cm^{-3}, and not necessarily equal.

11. The interband tunnel diode as recited in claim 1, wherein the thickness of the top and bottom spacer layers are between 0 and 50 nm, and not necessarily equal.

12. The interband tunnel diode as recited in claim 1, wherein the thickness of the top and bottom spacer layers are between 0 and 10 nm, and not necessarily equal.

13. An interband tunnel diode, comprising:

a bottom injector;

a bottom spacer;

a top spacer;

a top injector formed adjacent to, but not necessarily in direct contact with, the bottom injector, the bottom injector and top injector layers forming a p-n junction;

a material inserted between the bottom injector and top injector which serves as a tunnel barrier; and

wherein a first quantum well is formed adjacent to, but not necessarily in direct contact with, the bottom injector layer and the tunnel barrier.

14. The interband tunnel diode as recited in claim 13, wherein the quantum well is formed by an energy band offset at, or near, a heterojunction.

15. The interband tunnel diode as recited in claim 13, wherein the quantum well is formed by a highly doped layer.

16. The interband tunnel diode as recited in claim 13, wherein the quantum well is formed by a δ-doped layer.

17. The interband tunnel diode as recited in claim 13, wherein the quantum well leads to a resonant tunneling between said quantum well and the opposite polarity injector layer.

18. The interband tunnel diode as recited in claim 13, wherein the layers in the interband tunnel diode are a semiconductor or insulator.

19. The interband tunnel diode as recited in claim 13, wherein the layers in the interband tunnel diode are a Si compatible material.

20. The interband tunnel diode as recited in claim 13, wherein the layers in the interband tunnel diode are comprised of a Group IV alloy.

21. The interband tunnel diode as recited in claim 13, wherein the layers in the interband tunnel diode are comprised of, but not limited to, Si, Ge, C, Sn, $Si_{1-x}Ge_x$, $Si_{1-x}C_x$, $Si_{1-x}Sn_x$, $Si_{1-x-y}Ge_xC_y$, $Si_{1-x-y-z}Ge_xC_ySn_z$, $Si_{1-x}O_x$, $Si_{1-x}N_x$, $Al_{1-x}O_x$, or combinations thereof.

22. The interband tunnel diode as recited in claim 16, wherein the quantum well is doped above 10^{12} cm^{-2}.

23. The interband tunnel diode as recited in claim 16, wherein the quantum well is doped above 10^{13} cm^{-2}.

24. The interband tunnel diode as recited in claim 16, wherein the quantum well material is less than or equal to 10 nm thick.

25. The interband tunnel diode as recited in claim 16, wherein the quantum well material is less than or equal to 2.5 nm thick.

26. The interband tunnel diode as recited in claim 13, wherein the tunnel barrier material is doped below 10^{17} cm^{-3}.

27. The interband tunnel diode as recited in claim 13, wherein the tunnel barrier is less than or equal to 50 nm thick.

28. The interband tunnel diode as recited in claim 13, wherein the tunnel barrier is less than or equal to 10 nm thick.

29. The interband tunnel diode as recited in claim 13, wherein the doping concentrations of the top and bottom injector layers are between 1×10^{15} cm^{-3} and 5×10^{22} cm^{-3}, and not necessarily equal.

30. The interband tunnel diode as recited in claim 13, wherein the top and bottom spacer layers are doped below 10^{17} cm^{-3}, and not necessarily equal.

31. The interband tunnel diode as recited in claim 13, wherein the thickness of the top and bottom spacer layers are between 0 and 50 nm, and not necessarily equal.

32. The interband tunnel diode as recited in claim 13, wherein the thickness of the top and bottom spacer layers are between 0 and 10 nm, and not necessarily equal.

33. An interband tunnel diode, comprising:

a bottom injector;

a bottom spacer;

a top spacer;

a top injector formed adjacent to, but not necessarily in direct contact with, the bottom injector, the bottom injector and top injector layers forming a p-n junction;

a material inserted between the bottom injector and top injector which serves as a tunnel barrier;

wherein a first quantum well is formed adjacent to, but not necessarily in direct contact with, the bottom injector layer and the tunnel barrier; and

wherein a second quantum well is formed adjacent , but not necessarily in direct contact with, the bottom injector layer and the tunnel barrier.

34. The interband tunnel diode as recited in claim 33, wherein the first and second quantum wells are formed by an energy band offset at, or near, a heterojunction.

35. The interband tunnel diode as recited in claim 33, wherein the first and second quantum wells are formed by a highly doped layer.

36. The interband tunnel diode as recited in claim 33, wherein the first and second quantum wells are formed by a δ-doped layer.

37. The interband tunnel diode as recited in claim 33, wherein the first and second quantum wells lead to a resonant tunneling between said quantum wells.

38. The interband tunnel diode as recited in claim 33, wherein the tunnel barrier is formed between the bottom and top injector layers, wherein the first and second quantum wells are formed adjacent to the tunnel barrier.

39. The interband tunnel diode as recited in claim 33, wherein the layers in the interband tunnel diode are a semiconductor or insulator.

40. The interband tunnel diode as recited in claim 33, wherein the layers in the interband tunnel diode are a Si compatible material.

41. The interband tunnel diode as recited in claim 33, wherein the layers in the interband tunnel diode are comprised of a Group IV alloy.

42. The interband tunnel diode as recited in claim 33, wherein the layers in the interband tunnel diode are comprised of, but not limited to, Si, Ge, C, Sn, $Si_{1-x}Ge_x$, $Si_{1-x}C_x$, $Si_{1-x}Sn_x$, $Si_{1-x-y}Ge_xC_y$, $Si_{1-x-y-z}Ge_xC_ySn_z$, $Si_{1-x}O_x$, $Si_{1-x}N_x$, $Al_{1-x}O_x$, or combinations thereof.

43. The interband tunnel diode as recited in claim 36, wherein the first and second quantum wells are doped above 10^{12} cm^{-2}, and not necessarily equal.

44. The interband tunnel diode as recited in claim 36, wherein the first and second quantum wells are doped above 10^{13} cm^{-2}, and not necessarily equal.

45. The interband tunnel diode as recited in claim 36, wherein the first and second

quantum well material is less than or equal to 10 nm thick, and not necessarily equal.

46. The interband tunnel diode as recited in claim 36, wherein the first and second quantum well material is less than or equal to 2.5 nm thick, and not necessarily equal.

47. The interband tunnel diode as recited in claim 33, wherein the tunnel barrier material is doped below 10^{17} cm^{-3}.

48. The interband tunnel diode as recited in claim 33, wherein the tunnel barrier is less than or equal to 50 nm thick.

49. The interband tunnel diode as recited in claim 33, wherein the tunnel barrier is less than or equal to 10 nm thick.

50. The interband tunnel diode as recited in claim 33, wherein the doping concentrations of the top and bottom injector layers are between 1×10^{15} cm^{-3} and 5×10^{22} cm^{-3}, and not necessarily equal.

51. The interband tunnel diode as recited in claim 33, wherein the top and bottom spacer layers are doped below 10^{17} cm^{-3}, and not necessarily equal.

52. The interband tunnel diode as recited in claim 33, wherein the thickness of the top and bottom spacer layers are between 0 and 50 nm, and not necessarily equal.

53. The interband tunnel diode as recited in claim 33, wherein the thickness of the top and bottom spacer layers are between 0 and 10 nm, and not necessarily equal.

54. A method of fabricating an interband tunnel diode, the method comprising the steps of:

layering a bottom injector;

layering a top injector adjacent to, but not necessarily in direct contact with, the bottom injector, the bottom injector and top injector layers forming a p-n junction; and

layering a material between the bottom injector and top injector which serves as a tunnel

barrier.

55. A method of fabricating an interband tunnel diode, the method comprising the steps of:

layering a bottom injector;

layering a bottom spacer;

layering a top spacer;

layering a top injector adjacent to, but not necessarily in direct contact with, the bottom injector, the bottom injector and top injector layers forming a p-n junction; and

layering a material between the bottom injector and top spacers which serves as a tunnel barrier.

56. A method of fabricating an interband tunnel diode, the method comprising the steps of:

layering a bottom injector;

layering a bottom spacer;

layering a top spacer;

layering a top injector adjacent to, but not necessarily in direct contact with, the bottom injector, the bottom injector and top injector layers forming a p-n junction; and

layering a material between the bottom injector and top injector which serves as a tunnel barrier; and

wherein a quantum well is formed adjacent to, but not necessarily in direct contact with, the bottom injector layer and the tunnel barrier.

57. A method of fabricating an interband tunnel diode, the method comprising the steps of:

layering a bottom injector;

layering a bottom spacer;

layering a top spacer;

layering a top injector adjacent to, but not necessarily in direct contact with, the bottom

injector, the bottom injector and top injector layers forming a p-n junction; and

layering a material between the bottom injector and top injector which serves as a tunnel barrier;

wherein a first quantum well is formed adjacent to, but not necessarily in direct contact with, the bottom injector layer and the tunnel barrier; and

wherein a second quantum well is formed adjacent , but not necessarily in direct contact with, the bottom injector layer and the tunnel barrier.

58. The method of fabricating an interband tunnel diode as recited in claims 54, 55, 56, and 57, wherein the layers in the interband tunnel diode are grown epitaxially.

59. The method of fabricating an interband tunnel diode as recited in claims 54, 55, 56, and 57, wherein the layers in the interband tunnel diode are grown epitaxially, wherein the epitaxial layers in the interband tunnel diode are a semiconductor or insulator.

60. The method of fabricating an interband tunnel diode as recited in claims 54, 55, 56, and 57, wherein the layers in the interband tunnel diode are grown epitaxially, wherein the epitaxial layers in the interband tunnel diode are comprised of a Group IV alloy.

61. The method of fabricating an interband tunnel diode as recited in claims 54, 55, 56, and 57, wherein the layers in the interband tunnel diode are grown epitaxially, wherein the epitaxial layers in the interband tunnel diode are comprised of, but not limited to, Si, Ge, C, Sn, $Si_{1-x}Ge_x$, $Si_{1-x}C_x$, $Si_{1-x}Sn_x$, $Si_{1-x-y}Ge_xC_y$, $Si_{1-x-y-z}Ge_xC_ySn_z$, $Si_{1-x}O_x$, $Si_{1-x}N_x$, $Al_{1-x}O_x$, or combinations thereof.

62. The method of fabricating an interband tunnel diode as recited in claims 54, 55, 56, and 57, wherein the layers in the interband tunnel diode are grown in a molecular beam epitaxial (MBE) growth system.

63. The method of fabricating an interband tunnel diode as recited in claims 54, 55, 56, and 57, wherein the layers in the interband tunnel diode are grown in a chemical vapor deposition

(CVD) growth system.

64. The method of fabricating an interband tunnel diode as recited in claims 54, 55, 56, and 57, further comprising the step of heat treating the interband tunnel diode, during or after growth of the layers in the interband tunnel diode.

65. The method of fabricating an interband tunnel diode as recited in claims 54, 55, 56, and 57, further comprising the step of heat treating the interband tunnel diode, during or after growth of the layers in the interband tunnel diode, using an inert or reducing atmosphere, or moreover a reduction in ambient gas pressure at a temperature in the range of 300 to 1000°C.

66. The method of fabricating an interband tunnel diode as recited in claims 54, 55, 56, and 57, further comprising the step of heat treating the interband tunnel diode, during or after growth of the layers in the interband tunnel diode, using an inert or reducing atmosphere, or moreover a reduction in ambient gas pressure at a temperature in the range of 450 to 900°C.

67. The method of fabricating an interband tunnel diode as recited in claims 54, 55, 56, and 57, further comprising the step of heat treating the interband tunnel diode, during or after growth of the bottom quantum well layer in the interband tunnel diode.

68. The method of fabricating an interband tunnel diode as recited in claims 54, 55, 56, and 57, further comprising the step of heat treating the interband tunnel diode, during or after growth of the top and bottom quantum well layers, the top and bottom spacer layers, or the tunnel barrier in the interband tunnel diode.

69. The method of fabricating an interband tunnel diode as recited in claim 58, wherein the epitaxial growth system occurs over a substrate temperature range between 50°C and 900°C during growth of the layers in the interband tunnel diode.

70. The method of fabricating an interband tunnel diode as recited in claim 58 further comprising the step of lowering the substrate temperature before or during growth of the bottom injector layer in the interband tunnel diode.

71. The method of fabricating an interband tunnel diode as recited in claim 58 further comprising the step of lowering the substrate temperature before or during growth of the bottom quantum well in the interband tunnel diode.

72. The method of fabricating an interband tunnel diode as recited in claim 58 further comprising the step of elevating the substrate temperature before or during growth of the bottom injector layer in the interband tunnel diode.

73. The method of fabricating an interband tunnel diode as recited in claim 58 further comprising the step of elevating the substrate temperature before or during growth of the bottom quantum well in the interband tunnel diode.

74. A method of fabricating an interband tunnel diode by heat treating, during or after growth of the layers in the interband tunnel diode.

75. A method of fabricating an interband tunnel diode as recited in claim 74 by heat treating the diode using an inert or reducing atmosphere, or moreover a reduction in ambient gas pressure.

76. A method of fabricating an interband tunnel diode as recited in claim 74 by heat treating the diode at a temperature in the range of 300 to 1000°C.

77. A method of fabricating an interband tunnel diode as recited in claim 74 by heat treating the diode at a temperature in the range of 450 to 900°C.

78. A method of fabricating an interband tunnel diode as recited in claim 74 by heat treating the diode at a temperature in the range of 600 to 800°C.

79. A method of fabricating an interband tunnel diode as recited in claim 74 by heat treating the diode for up to 6 hours.

80. A method of fabricating an interband tunnel diode as recited in claim 74 by heat treating the diode for up to 1 hour.

81. A method of fabricating an interband tunnel diode as recited in claim 74 by heat treating the diode for up to 10 minutes.

82. A method of fabricating an interband tunnel diode as recited in claim 74 by heat treating the diode for up to 2 minutes.

83. A method of fabricating an interband tunnel diode by growing at least one quantum well epitaxially at reduced substrate temperature.

84. A method of fabricating an interband tunnel diode as recited in claim 83 by growing at least one quantum well epitaxially while maintaining a substrate temperature between 0°C and 900°C.

85. A method of fabricating an interband tunnel diode as recited in claim 83 by growing at least one quantum well epitaxially while maintaining a substrate temperature between 20°C and 500°C.